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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,487	11/03/2000	Jean-Didier Allegrucci	003242.P015	7643

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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/705,487	ALLEGRUCCI, JEAN-DIDIER	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

In regards to applicants argument that Rieken does not disclose nor suggest accessing the static state of the programmable hardware through the debug port. This is clearly incorrect see column 4 line 50 to column 5 line 25.

In regards to applicants argument that Jones does not teach stopping the system clock such that the state of the programmable hardware is held static: Jones teaches column 9 lines 23-25 that asserting the suspend pin stops all CPU's on the chip. It does not expressly state that the stopping of the CPU includes stopping the clock to the CPU this is the standard method of stopping a CPU, and Rieken expressly teaches stopping a clock.

In regards to applicants argument that Jones does not teach accessing the static state of the programmable hardware through the debug port. Jones teaches Column 9 lines 51-50, that a static state of the CPU (stored into a dedicated shadow register) is accessed through the debug port.

The examiner notes that the "static state" in Jones is not the "state of the programmable hardware is held static". It is however clear that the applicants claim language was meant to indicate that the "static state" and the "state of the programmable hardware is held static" were the same static state. The previous examiner erred in not giving a 35 U.S.C 112,2nd for lack of antecedent bases for "the static state". The examiner will further address these two states as the same.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 1, 7 and 13 recites the limitation "the static state". There is insufficient antecedent basis for this limitation in the claim. It is clear from applicants arguments and the "state of the programmable hardware is held static" is meant to be the static state. amending "held static" to read "held in a static state" would alleviate this rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mehring PN 5,675,729 in view of Jones et al PN 6,356,960.

In regards to claims 1-2, 7-8: Mehring teaches a method for diagnosing programmable hardware comprising: recognizing an occurrence of a user-specified event (events) generating a signal to cease bus access (Stop clock signal), in a configurable system on a chip, upon the

occurrence of the user specified event, the signal generated by a breakpoint unit (Breakpoint trigger logic), such that the user-specified event of the breakpoint unit can be programmed through a debug port (Jtag port); stopping the system clock such that the state of the programmable hardware is held in a static state (stop clock performed); and accessing the static state of the programmable hardware through the debug port (a scan). Mehring does not expressly teach the claimed structure of the computer system or that the bus transactions are allowed to complete. The examiner notes Mehring teaches the system is a system on a chip. Jones teaches applicants claimed structure of the configurable system on a chip integrating at least a central processing unit (CPUO 12 and 13), an internal system bus (e.g. p-link 15 or pipeline) and a configurable logic (e.g. event logic 44) and allowing completion of all pending bus transactions (causes a CPU to drain the execution pipelines; col. 9, lines 35- 384 col. 10, lines 15-18). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Jones system structure in the tested system of Mehring because this would have provided for a simple system structure. It would have been obvious to a person of ordinary skill in the art at the time of the invention to allow completion of all pending bus transactions because this would have prevented data corruption upon restarting of the system.

As per claims 3 and 9, wherein the debug port is a bus master would be within the teachings of Mehring-Jones in that Jones discloses external debugging device is operable to transmit control signals through the debugging port to stop CPU execution; to load a debugging routine to be executed by the CPU; and to restart operation of the CPU. Essentially, the external

debugging device masters over the p-link bus through the debugging port to perform the above stated functions. Therefore, the debug port is a bus master (Abstract).

As per claims 4 and 10, Mehring-Jones teaches "wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions" (e.g. Jones: col. 9, lines 35-38.

As per claims 5 and 11, Mehring-Jones teaches "wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions" (e.g. Jones: col. 9, lines 35-38; Additionally, Mehring teaches the generation of a clock stop cycle).

As per claims 6 and 12, Both Mehring and Jones teaches wherein the specified event is programmed by a user.

As per claims 13 and 14, Both Mehring and Jones discloses the claimed invention including an apparatus comprising: means to recognize an occurrence of a user-specified event; Jones teaches means to cease bus access (col. 9, lines 15-26; col. 12, lines 12-18) in a configurable system on a chip (computer system on integrated chip; Abstract), upon the occurrence of the user-specified event, the configurable system on a chip integrating at least a central processing unit (CPU0 12 and 13), an internal system bus (e.g. p-link 15 or pipeline) and a configurable logic (e.g. event logic 44); means to allow completion of all pending bus

transactions (e.g. including event logic 44 causes a CPU to drain the execution pipelines; col. 9, lines 35-38; col. 10, lines 15-18); Mehring and Jones teach means to stop the system clock (Stop clock signal from Mehring or event logic 44, stops all CPU execution or CPU is suspended; col. 9, lines 23-26 from Jones) such that the state of the hardware is held static; and means to access the static state of the hardware through a debug port (Jtag port) [e.g. including external debugging device; see col. 9, lines 50-55].

As per claim 15, Mehring-Jones teaches wherein the debug port is a bus master would be within the teachings of Jones in that Jones discloses external debugging device is operable to transmit control signals through the debugging port to stop CPU execution; to load a debugging routine to be executed by the CPU; and to restart operation of the CPU. Essentially, the external debugging device masters over the p-link bus through the debugging port to perform the above stated functions. Therefore, the debug port can be seen as a bus master (Abstract).

As per claim 16, Mehring-Jones teaches wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions (e.g. Jones: col. 9, lines 35-38; Additionally.

As per claim 17, Mehring-Jones teaches wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions (e.g. Jones: col. 9, lines 35-38; Additionally, Mehring teaches the generation of a clock stop cycle).

As per claim 18, Mehring and Jones both teach wherein the specified event is programmed by a user.

As per claims 19-21, Mehring and Jones both teach wherein the user-specified event comprises a sequence of events (e.g. see Jones: cols. 9-12).

Allowable Subject Matter

7. Claims 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record do not teach or suggest a breakpoint unit connected to a plurality of buses such that the breakpoint unit generates a signal in response to a user-specified event on any of the plurality of buses. Claim 23 is dependent from claim 22, hence it is also allowable for the same reasons.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM
February 15, 2005

PAUL R. MYERS
PRIMARY EXAMINER